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Low voltage low power programmable logic gate based on SE-MOSFET

By

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Abstract:

Single electron transistor (SET) is one of the most promising devices for nano-scale circuit design. In this paper, new low voltage low power programmable logic gate circuits using SE-MOSFET are presented. Devices that combine single-electron and metal–oxide–semiconductor (MOS) transistors allows compact realization of basic logic function that exhibit periodic transfer characteristics. The proposed SE-MOSFET logic gates are useful for implementing binary logic circuits. The proposed programmable logic gate is verified by simulating the circuit using PSPICE. The results show that the operation of proposed circuit is in accordance with the theories.

Keywords:

SE-MOSFTT Hybrid Circuits, Low Power Circuits, Logic Gate.

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1. Introduction:

Recent progress in Si LSIs has made it possible to Miniaturize devices, especially the gate length of MOSFETs, to the order of 10-nm. This not only makes device fabrication difficult but also makes it difficult to attain high performance. Another difficulty in current LSIs is increasing power dissipation in a small Si chip.

Single-electron transistors (SETs) are very attractive for digital logic applications because they have the key advantages such as ultra small size, ultra low power consumption and new functionalities due to Coulomb oscillation and Coulomb blockade [1,2]. However, there are particular obstacles for implementing SET logic gates, such as low voltage gain, high output impedance, and sensitivity to background To overcome the inherent disadvantages of SETs, various types of hybrid circuits combining SETs with metal–oxide–semiconductor field-effect transistors (MOSFETs), SET-MOSFET hybrid circuits, have been proposed [3–6]. The use of SETs combined with MOS transistors [3,7] allows compact realization of basic logic functions that exhibit periodic transfer characteristics, whose amplitude, period and phase can be programmed independently. This unique property is particularly useful for implementing binary logic circuits, MV logic circuits and binary-MV mixed-mode logic circuit

2. *Principle of Operation:*

The SET is the most fundamental of various single-electron devices. The SET must have a small conductive island to exploit the Coulomb blockade for manipulating electrons by means of one-by-one transfer.

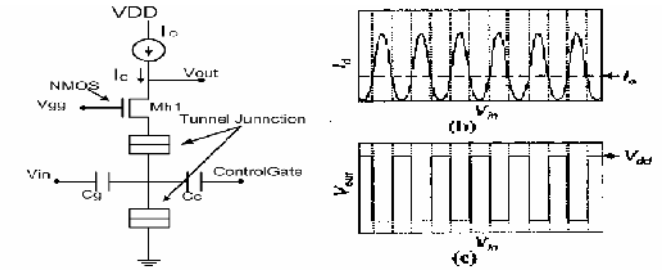

Figure.1 The universal literal gate comprising a SET, a MOSFET and a constant-current (CC) load Io.

Fig.1(a) is a schematic of the universal literal gate comprising a SET, a MOSFET and a constant-current (CC) load Io . A MOSFET with a fixed gate bias of Vgg is used here to keep the SET drain voltage almost constant at Vgg– Vth, where Vth is the MOSFET threshold voltage. This (Vgg–Vth) is set low enough to sustain the Coulomb-blockade condition. Current through this circuit increases and decreases periodically as a function of input voltage [Fig.1(b)] unless the CC load is connected. The current is determined only by the input voltage; it is independent of the output Voltage, because the drain voltage of the SET is kept constant by the MOSFET. When the CC load is connected and the increasing drain current crosses the load line Io of the output voltage switches very sharply from high to low. Then on the other hand, when the decreasing drain current crosses the load line, the output voltage switches from low to high. And so on. Thus, sharp square-wave-like input–output characteristics with a large voltage swing are obtained [Fig.1(c)]. The output Vout becomes logic 1 when the SET is off and Vout becomes logic 0 when the SET is on. The periodic waveform of the output is shifted by half period applying a constant dc voltage Vctl=e/Cc {V}, where Cc is the control of the control gate the waveform shift due to the control–gate potential as illustrated in fig.1 (b). So the circuit in fig.1(a) can be used as an inverter if Vpg=0, used as a buffer if Vpg=1 and used as XOR}}}}}}}}if Vpg=Vin2 the output will be Vout=Vin1⊕Vin2

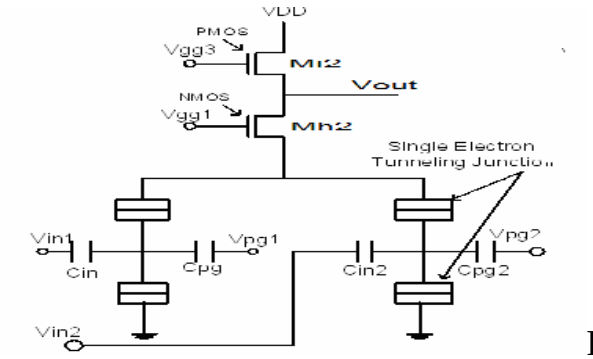

Figure.2 The parallel gate

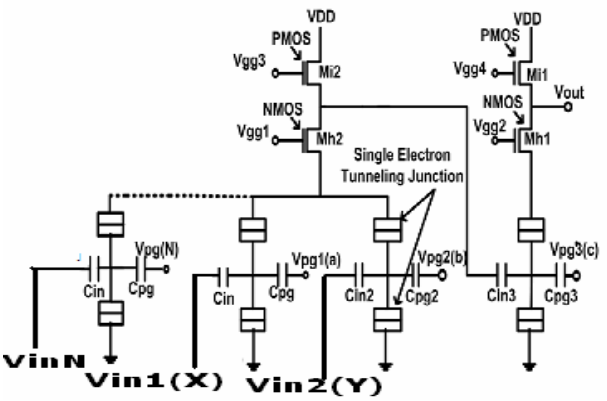

Figure.3 Proposed logic circuit.

When we use parallel gate as show in figure2 We have two control gate and

Vout {Vin1.Vin2 If Vg1=1 and Vg2=1

$\overline{Vin1}$.Vin2 If Vg1=0 and Vg2=1

$\overline{Vin1.Vin2}$ If Vg1=0 and Vg2=0

Vin1.$\overline{Vin2}$ If Vg1=1 and Vg2=0

3.Proposed Programmable Logic Circuit

In this paper we construct programmable logic circuit that consists of two blocks, the first blocks, is the parallel gate in fig.2 (a) and the second blocks, is the literal gate in fig.1 (a) where *X* and *Y* are input signals. Fig.3(*a*) shows a schematic diagram of a programmable logic circuit using the SE-MOSFET hybrid circuits. In the parallel gate circuit, the two gate used as input gates and the other two gates used as control gates. In the lateral gate one of the two gates is connected to the out put of the parallel gate and the second gate used as control gate. When the two inputs of programmable logic circuit to the inputs X and Y, and the control gates to the control voltages A,B and C as shown in Fig.4, there are possible twelve function for the circuit corresponding to the parameters (A,B ,C) as show in fig.4.

4.Simulation Results

Figures (5-7) show the simulation results of the proposed of a programmable logic circuit Here the tunneling resistances of drain and source junction in the SET *R*d =Rs = 100 k, capacitances of drain and source junction in the SET Cd = Cs =0.18aF, gate capacitances in the SET Cg1=Cg2 =0.27aF and temperature T = 100 K. the enhancement-mode PMOSFETs Mi1, Mi2, are used as the current source, and the gate width and length of the enhancement-mode PMOSFETs are .1 μm and 0.1 μm, respectively. .The gate width and length of the enhancement-mode NMOSFETs, *M*h1 , Mh2, are 0.1 μm and 0.1 μm, respectively. The Bias voltage (Vgg) of the enhancement-mode NMOSFET gate is 0.49 V. The other parameter is V_{DD} = 0.9 V. But of course we need to address many technical limitation As Set's are made smaller, there is an increase in the operating temperature, the operating frequency, and the device packing density. These are desirable consequences of the shrinking of SET devices. The undesirable consequences of the shrinking of Set's are that the electric fields increase, the current densities increase, the operating voltage increases, the energy dissipated per switching event increases, and the power dissipated per unit area increases, the voltage gain decreases, the charge gain decreases, and the number of Coulomb oscillations that can be observed decrease. Fig.5 shows the simulated waveforms of

the input signal X, input signal *Y*, and the output of each case. Fig.6 shows the simulated waveforms of the input signal *X*, input signal Y, and the output when we connect the two inputs in the parallel gate by each other (X and Y).

We can increase the number of inputs by increase number of parallel SET as show in fig.3.

fig.7 shows the simulated waveforms of four inputs.

5. Conclusion

In this paper, we proposed basic SET logic gates useful for designing a programmable logic circuit that operate all combination logic circuit by change the potential voltage of the Control –gate The proposed a programmable logic circuit seems useful in many applications, where low-power area-efficient circuit implementation of mixed-signal interface is essential. Such applications may include logic-in-memory circuits, functional memory systems, Field-Programmable Gate Arrays (FPGAs), computational sensors with on-chip signal processing capability (such as computational image sensors and intelligent chemical/biological sensors), advanced smart dust, signal processors for mobile devices, etc

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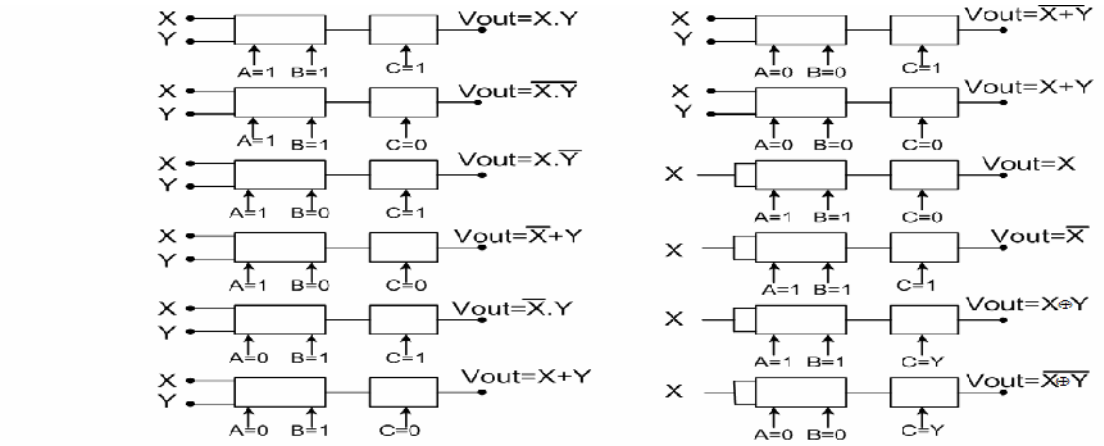
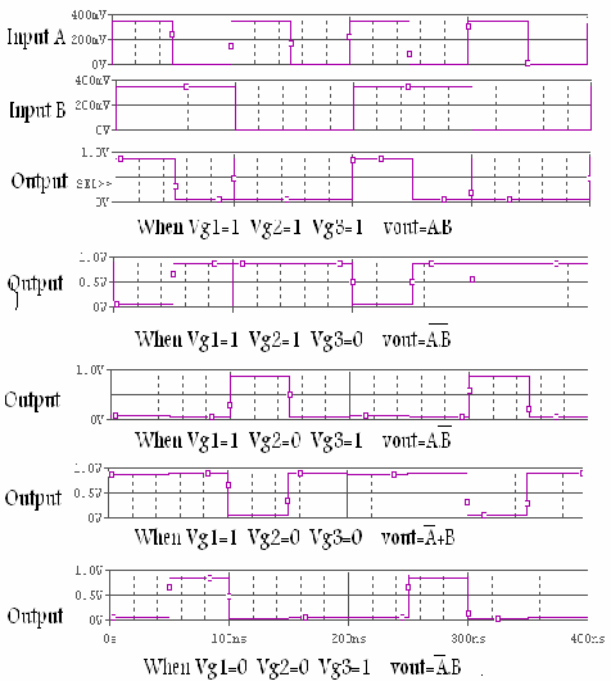


Figure.4 The possible twelve function



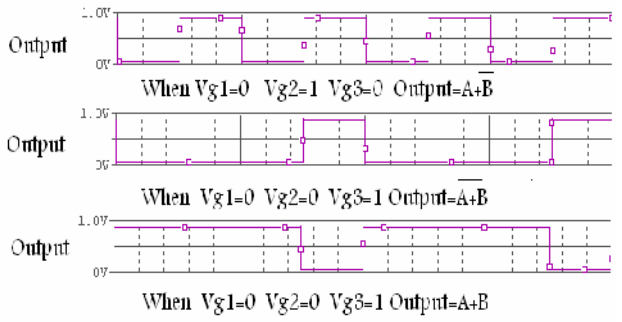


Figure 5 The simulated waveforms of the input signal X, input signal *Y*, and the output of each case.

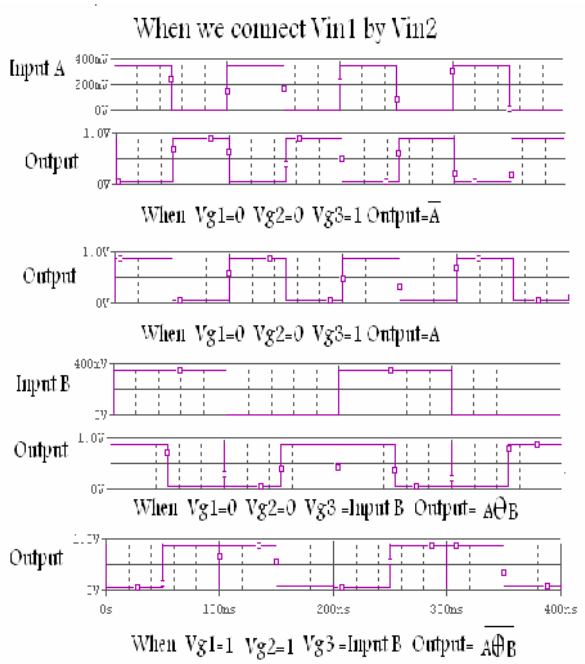


Figure 6 The simulated waveforms of the input signal *X*, input signal Y, and the output when we connect the two inputs in the parallel gate by each other (X and Y).

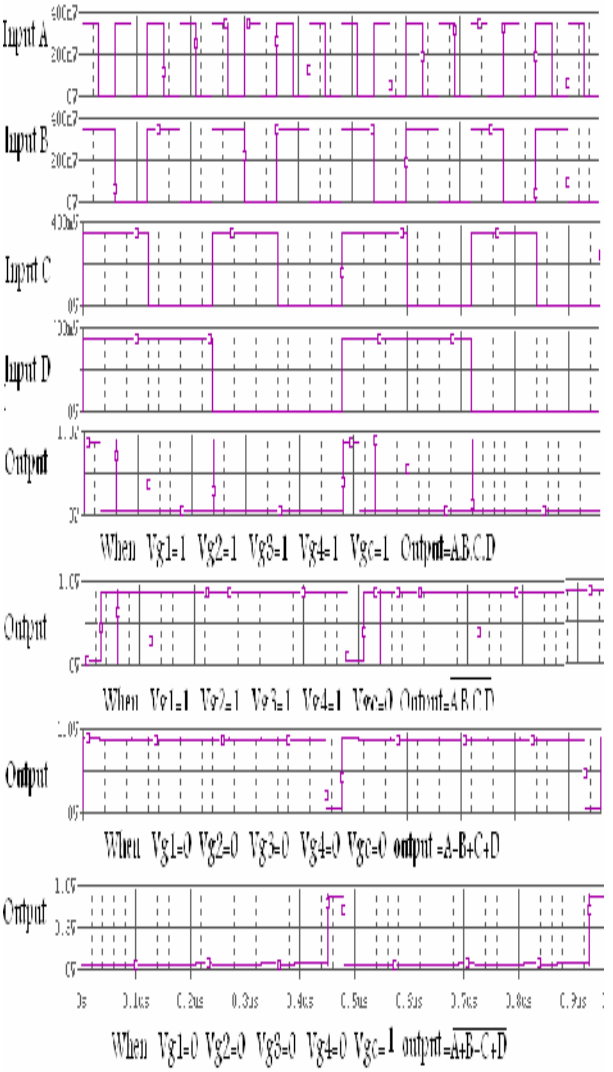


Figure 7 The simulated waveforms of four inputs.