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Low power, Low Voltage and High Gain UWB Low-Noise Amplifier in the 0.13 µm CMOS technology

By

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Abstract:

In this paper, we present a fully integrated CMOS LNA (low noise amplifier) with input matching LC ladder technique circuitry to cover the upper band of UWB from 3.1 to 10 GHz. Also, an improved technique of derivative superposition (DS) method is proposed to improve the linearity by using both forward body bias technology, and current-reused. The proposed LNA can operate at reduced supply voltage and power consumption. This configuration provides better input matching, lower noise figure, and more reverse isolation which is vital in LNA design. Complete analytical simulation of the circuit results in frequency of 3.1 GHz to 10 GHz, with 2.44 dB NF_{MIN}, 50Ω input impedance, 13.5dB peak power gain (S_{21}), high reverse isolation (S_{12}) -50 dB, -15dB input matching (S_{11}) and -10dB output matching (S_{22}), while dissipating as low power as1.5mW low supply voltage of 0.6 V.

Keywords:

CMOS, forward body bias, low noise amplifier (LNA), low voltage, Noise figure (NF), nonlinearity, third-order input intercept point (IIP_3)

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1. Introduction:

Portable applications such as WLAN transceivers, cell phones, and sensor networks strive to meet stringent performance requirements with the lowest power consumption to preserve battery life. The most efficient technological approach for reducing power consumption is through power supply voltage scaling, but conventional cascade topology [1] has been widely used in low noise amplifier (LNA) circuit design to optimize circuit performance such as high gain, and high reverse isolation. Nevertheless, it is not suitable for low-voltage applications because the supply voltage must be larger than twice the threshold voltage (v_{th}) of the transistors.

LNA circuit topologies have been devised to yield a low voltage supply (V_{dd})[2] using a folded-cascode LNA suitable for low-voltage, low-power this structure utilizes the complementary nature of CMOS, employing both NMOS and PMOS transistors to reduce the required voltage. However, the work conducted thus far has suffered from low linearity and as we know the mobility of PMOS is less than the mobility of NMOS so that, this design at fast operations

Linearity is a key performance parameter for RF circuits since nonlinearity may cause harmonic generation, gain compression, desensitization, blocking, cross modulation, inter-modulation distortion and many other problems. The linearity of the LNA is usually specified as an input-referred third-order intercept point (IIP_3) in recently papers [3],[4] provide two different techniques to improve the linearity derivative superposition (DS) which will discuss later and using folded PMOS I_{MD} sinker but this two methods doesn't take in its account the noise figure as it used additional transistor .

For the low-noise amplifier (LNA), high linearity, and low power consumption should be achieved without lowering other performances, such as low noise figure (NF), high gain, and good impedance matching

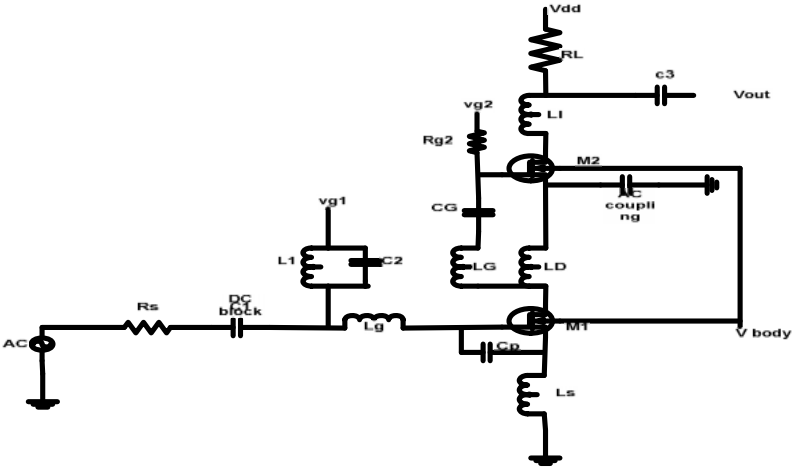

Figure (1): *Schematic of the proposed LNA.*

2 Circuit Architecture And Design

Figure (1) shows the complete circuit of the proposed low noise amplifier which we will explain in details its techniques

I- Input matching

Using LC ladder theory [2], The LC network presented in Figure (2) is a second order pass band filter that's the impedance response Z_{in} is depicted in Figure (3) Hence Z_{in} is purely resistive and equal to:

$$R_{eq} = \frac{g_m L_s}{C_{gs}} + r_g \approx w_T L_s \qquad (1)$$

where w_T The unity-current gain angular frequency of the MOSFET

$$w_T \approx \frac{g_m}{C_{gs}} = \frac{3\alpha\mu V_{eff}}{2 L^2}$$

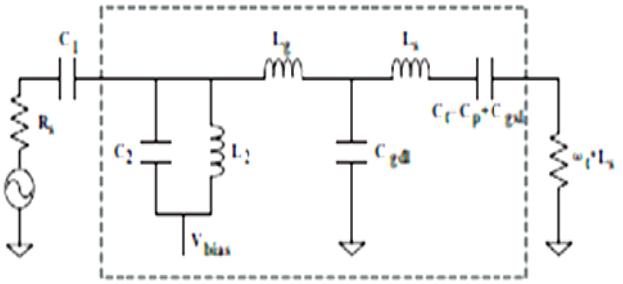

Figure (2): *Schematic of LNA input match network*

Within a frequency range defined as follows

Figure (3): *band pass width of match network* [7]

$$f_L = \frac{1}{2\pi RC_2} \approx \frac{1}{2\pi L_1} \quad (2)$$

$$f_U = \frac{1}{2\pi RC_1} \quad (3)$$

And for output matching is used a series RLC with a resonance frequency the center of the band (6.5GHz) and less quality factor to increase the bandwidth

II-The low voltage supply

The cascade LNA is widely used in LNA designs but it not suitable for low voltage applications due to stacking configurations, in the stacking structure the supply voltage must be larger than $2v_{th}$ to prevent transistors with low supply voltage in the weak inversion region from inducing NF and gain performance degradations. Forward body bias technology [3] is also introduced to come over this problem. The well-known threshold

$$v_{th} = v_{tho} + (\sqrt{v_{be} - 2\Phi_f} - \sqrt{2\Phi_f}) \quad (4)$$

Where v_{tho} is the threshold voltage without bulk-source voltage i.e. v_{bs}=0, γ is the bulk threshold parameter, and ϕ_f is the bulk Fermi potential.v_{th} could be reduced by applying forward body bias. Furthermore, the body of each NMOS transistor is biased at 0.52 V and is much lower than the P-N junction turn-on voltage, that is, the bulk-to-source voltage should be smaller than 0.7 V. The introduced body leakage current could then be negligible and when v_{bs} =0.52 the vth become less than 0.3 v when vtho=0.45 v.

III. High linearity technique

The nonlinearity of a MOS transistor arises from its voltage-to-current (V–I) conversion. The drain current in a MOSFET can be modeled in terms of its gate–source voltage as follows

$$i_d = g_1 v_{gs} + g_2 v_{gs}^2 + g_3 v_{gs}^3 + \cdots \cdots \quad (5)$$

where g_{m1} is the main transconductance, represents its g_{m2} second-order nonlinearity obtained by the second-order derivative of MOSFET dc transfer characteristics (I_d–v_{gs}) and g_{m3} is the third-order nonlinearity obtained by the third-order.

$$IIP3 = \sqrt{\frac{4\, g_{m1}}{3\, g_{m3}}} \qquad (6)$$

In previous papers [4], implementation of a high linear LNA using the improved DS method is proposed. The input stage is formed by two transistors connected in parallel as shown in Figure (4).

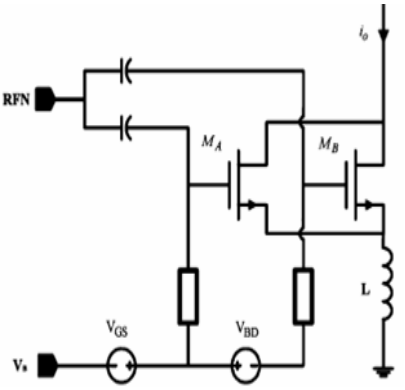

Figure (4): *principle the derivative superposition method*

One transistor is biased in the strong inversion region and another one is biased in the moderate inversion region, thus allowing a feasible source degeneration inductance at the sources of the two transistors while keeping high IIP_3 improvement with the DS method

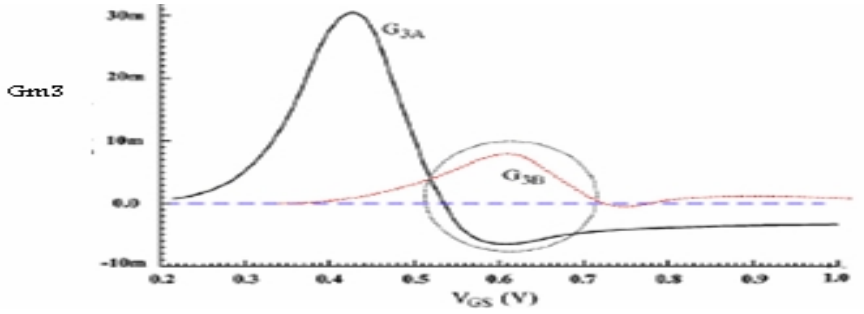

Figure (5): *The third-order nonlinear coefficient g_{m3A} and g_{m3b} of M_A and M_B versus the voltage source V_{GS}* [3]

As shown Figure (5) the third-order nonlinear coefficient g_{m3A} and g_{m3b} of M_A and M_B

versus the voltage source V_{GS}. By setting the voltage source V_{BD} to 0.3 V, M_A is designed to work in the strong inversion region and M_B is designed to work in the moderate inversion region. g_{m3} Is defined as

$$g_{m3} = \frac{1}{6}\frac{\partial^3 I_D}{\partial v^3_{Gs}} \qquad (7)$$

And controls the third-order inter-modulation distortion (I_{MD3}) at low signal levels, thus determines IIP_3. It could be seen that the third-order nonlinear coefficient g_{m3A} of the transistor in the strong inversion region is negative and the third-order nonlinear coefficient g_{m3b} of the transistor in the moderate inversion region is positive. The negative g_{m3A} is aligned with the positive g_{m3b}, but they have a similar mirror-image curvature, the resulting composite g_{m3} will be close to zero and the theoretical IIP3 will be significantly improved in a relatively wide range of the gate biases. But in my design I used only one transistor (A) with biasing at v_{GS} =0.55 v where the $g_{m3A} \approx$ zero using only one transistor is better than using two transistor as it low cast, low area, low power, and low noise figure. But this technique will provide a low power gain, so to come over this problem cascade topology (two stage amplifiers) is used. But it will increase the power dissipation. This problem will be come over using current reused technique.

IV. Current-Reused Technique

The current-reused configuration [6] can be considered as a two stage cascade amplifier, where the first stage is the CS amplifier, and the second stage is the cascode amplifier as shown in Figure (6)

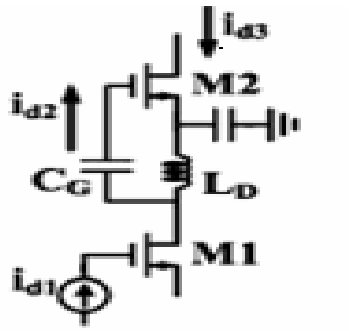

Figure (6): *principle of current reuse technique*

The purpose of using L_G and C_G is to perform a series-resonant with C_{GS} of a M_1 for

low impedance path, while the impedance of L_D is adequately large in the desired bandwidth to provide a high impedance path to block the signal.

$$\frac{i_{d2}}{i_{d1}} = \frac{g_{m1}}{s(C_{gs1} + C_{gd1})} \tag{8}$$

$$\frac{i_{d3}}{i_{d2}} = \frac{g_{m2}}{s(C_{gs2} + C_{gd2})} \tag{9}$$

Combining (9) and (10), it can be seen that the input signal is amplified twice under the same dc current for achieving high gain under low power consumption.

3. simulations result and discussion

The proposed circuit was simulated using ADS2008 (advanced design system2008) in 0.13µm TSMC CMOS process, Figure (7) shows that the noise figure (NF) is <-5dB within the range (5GHz to 9.3GHz), Figure(8) shows that the design provide forward power gain (S21) 22.17dB at 3.6 GHz, Figure(9) shows that the design give a good input matching (S11)for all frequency more than 4 GHz and Figure(10), Figure (11) show that the circuit operate at good output matching and low reverse transmission gain.

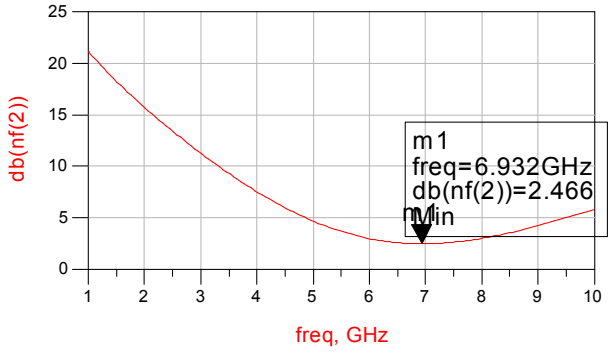

Figure (7): *simulated NF.*

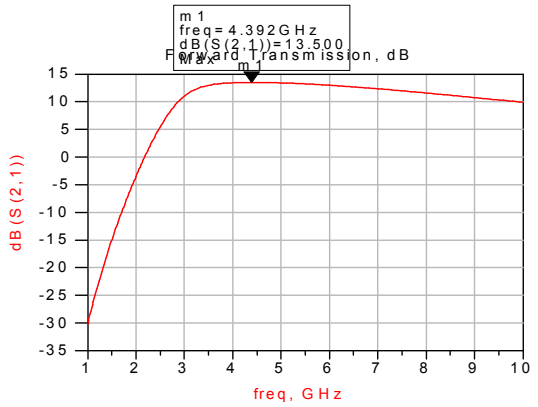

Figure (8): *Simulated power gain.*

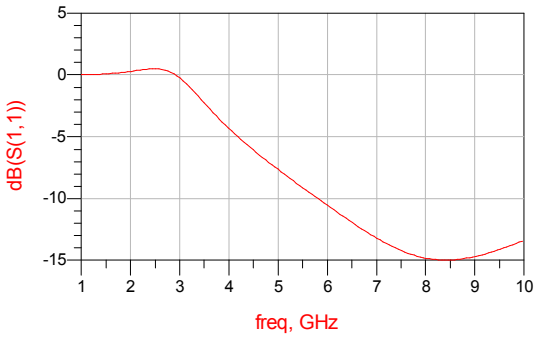

Figure (9): *simulated input matching.*

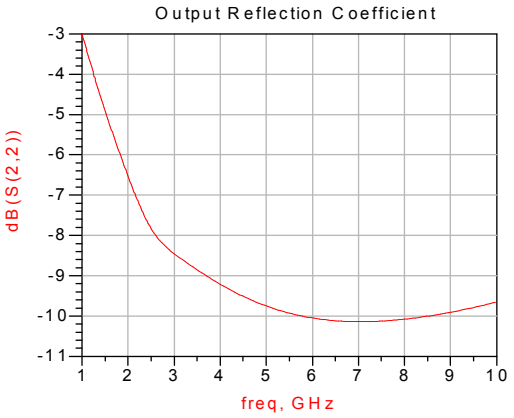

Figure (10): *Simulated output matching.*

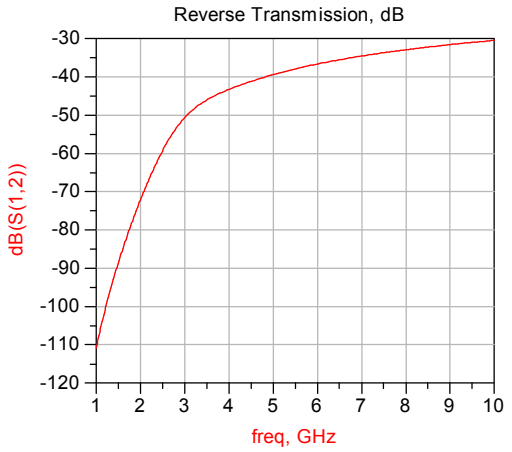

Figure (11): *simulated reverse gain*

The stability calculations below show that transistor is unconditionally stable since k>1

$$k = \frac{1 - |s_{11}|^2 - |s_{22}|^2 + |\Delta|^2}{2|s_{12}s_{21}|} \qquad (10)$$

where $\Delta = s_{11}s_{22} - s_{12}s_{21}$

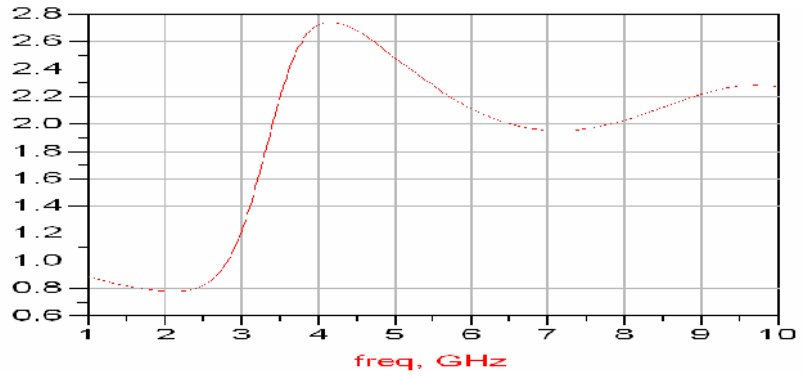

Figure (11): *stability factor (k)*

Table (1): *Performance summary and comparison with published works*

Specification	This work	[8]	[9]	[10]	[11]	[12]	[13]
Technology	0.13-µm CMOS	0.18-µm CMOS	0.18-µm CMOS	0.18-µm CMOS	0.13-µm CMOS	0.18-µm SiGeHBT	0.18-µm CMOS
Frequency (GHz)	3.1-10	3.1– 10.6	3.1– 10.6	3.1 – 10.6	3.1 – 10.6	3.1 – 10.6	3.1 – 10.6
Inputs return loss S_{11} (dB)	<-9	< -9	< -10	< -11	< -10	< -14	< -8
Supply voltage(V)	0.6	1.8	1.8	1.5	1.2	2.5	1.8
Power gain (dB)	10-22.5	9.2	8.5	10.8-12	13.7-16.5	16.4-18	13.5-16
Noise figure (dB)	2.44-5	4 - 9	4.3 -5.3	4.7 - 5.6	2.1-2.8	3.4 - 4.7	3.1- 6
Bandwidth (GHz)	2.9-5.5	2.3 - 9.2	1.3 - 1.7	1 - 11.6	3.1-10.6	3 -10	3.4 -11.4
ReversegainS_{12} (dB)	<-25	< -35	No info	No info	< -30	No info	<-40
IIP3@6GHz(dBm)	-10.2	-6.7	-8	-11	-7	-11.7	-7
P_{diss} (mW)	1.5	9.2	4.5	10.6	9	42.5	11.9

4. conclusion

This paper presents fully integrated (3.1-10) GHz design integrated in a TSMC 0.13µm CMOS process requires only voltage of 0.6 V consuming 1.5 dc powers. The feasibility of a newly proposed wideband matching topology and current-reused technique for improving noise performance, achieving good input matching and high power gain. The proposed LNA provided a peak power gain of 13.5 dB. NF ranged from 2.4 dB to 5 dB within the bandwidth. This LNA can be used for low voltage and low power wireless applications. Future work may be focused on LNA design using current conveyer.

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