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ENHANCED PERFORMANCE OF COMPLEMENTARY GALLIUM ARSENIDE (CGAAS) CIRCUITS

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ABSTRACT :

The theory, design, implementation and evaluation of Two-Phase Dynamic FET Logic (TPDL), a logic family that is compatible with the existing Complementary Gallium Arsenide (CGaAs) fabrication process and design tools, is documented. Several different logic functions have been implemented in both TPDL and static logic. A performance comparison between the TPDL and static logic circuits is also performed. TPDL circuits are much faster than the static circuits performing the same function because the former do not use PFETs for logic expression evaluation, only for precharging. Also, TPDL circuits consumes less power than static circuits because they have no short-circuit current and a reduced leakage current. The maximum operating frequency of the TPDL circuits is 2.38 GHz and they have the lowest power-delay product ever reported in this technology (0.01mW/gate/MHz).

KEY WORDS :

TPDL , CgaAs , Dynamic Logic , VLSI and Domino Logic .

1. INTRODUCTION :

Complementary GaAs (CGaAs) fabrication technology is an evolution of GaAs E/D MESFET technology, much like the way CMOS is an evolution of NMOS technology. CGaAs has an advantage over CMOS in that it has no substrate contacts and no latchup possibilities, which reduce the layout area and increase the yield of CGaAs circuits. CGaAs is the lowest power digital technology that is practical for the frequency range of 300 MHz to 1 GHz and above [1]. This technology has already achieved 0.1mW/MHz/gate at 0.9 V. Complementary digital ICs can operate at speeds over 500 MHz. By sacrificing some power dissipation, a 1 GHz digital signal processor has been made with a speed/power measurement of 0.16 mW/MHz/gate [2]. The speed-power performance of 1 mm CGaAs has been shown to be superior to 0.5 mm CMOS or thin film SOI equivalents [2].

Dynamic logic circuits have been designed in CMOS to decrease the power consumption as well as to increase the maximum operating frequency. Another advantage of dynamic circuits is that they are non ratioed logic. Therefore, the transistor sizes can be minimized to reduce the layout area and power dissipation [3]. CGaAs dynamic logic circuits have been designed and implemented in the research described in this paper. The designed circuits include Domino logic, N-P Domino logic, and Two-Phase dynamic logic (TPDL). They have a higher speed than GaAs Directly Couple FET Logic (DCFL) and lower power consumption than

GaAs static complementary logic [1, 4]. The circuits designed in TPDL show much better performances than all the other studied dynamic circuits [5, 6, 7]. Therefore, only the performance of the designed TPDL circuits are shown in this paper.

2. THEORY OF OPERATION OF TPDL CIRCUITS :

TPDL circuits consist of two main stages, a f1 stage and a f2 stage, as shown in Figure 1. The clock phases f1 and f2 are non overlapped in the logic low level. Each stage consists of pass gates, a clocked precharge PFET, a clocked discharge NFET and a N-transistor logic block. The outputs of f1 stages are connected to the inputs of f2 stages and vise versa.

The detailed operation of the TPDL circuits is as follows; during f1 high and f2 low, the first stage is evaluated, the second stage is precharged and the output of the first stage is stored on the second-stage inputs. During f2 high and f1 low, the first stage is precharged, the second stage is evaluated and the output of the second stage is stored on the first-stage inputs. When both f1 and f2 are simultaneously high, both stages (f1 and f2) will be evaluated and their outputs will be isolated from the next stages by the off pass gates so there is no corruption of data. The two phases must be non overlapped in the low state as shown in Figure 1 to prevent data corruption. If this condition is not satisfied and both phases are low at the same time, both stages will precharge their output nodes and the precharged outputs will be passed to the inputs of the next stage. When either f1 or f2 switches to logic low, the corresponding stage will start to evaluate the erroneous inputs (pre-charged outputs of the previous stages) and give an erroneous output. If any input to a f1 (f2) stage is supplied from another

circuit (non-TPDL circuit), it has to be stable (unchanging) during f1 (f2) logic low. Another condition that must be satisfied is that f1 stage outputs can only be connected to f2 stage inputs and f2 stage outputs can only be connected to f1 stage inputs. This is similar to Si CMOS "zipper" logic.

Because of the use of pass gates in front of each evaluating logic block, TPDL designs are self latching and well suited for pipelined architectures. TPDL systems can be pipelined to reach the maximum operating frequency without having to add additional storage elements (pipeline registers).

3. CIRCUIT DESIGN :

Basic combinational logic gates (Inverter, NAND gate, NOR gate, XOR gate and XNOR gate), as well as sequential circuits (D Flip-Flop and Linear Feedback Shift Registers), are designed and implemented using the above circuit topology. An inverter, NAND gate and NOR gate are implemented here because they are the main building blocks of any logic family. Figure 2 shows the N-transistor logic block representation of these gates which is preceded by a pass gate for every input. Also, a four-bit carry lookahead adder and a polynomial multiplier have been designed and implemented. The same logic functions have also been designed using complementary static logic for performance-comparison reasons.

4. RESULTS AND COMPARISON :

The transistor model parameters used in this paper were supplied by Motorola and are representative of the devices manufactured by the Motorola CGaAs fabrication processes. These parameters were extracted from actual wafer probing data. The circuits presented here were simulated in HSPICE which has a

superior convergence and accurate modeling features. The layout parasitic capacitance are minimal because of the small layout area of the test circuits. Therefore, the simulation results should not deviate significantly from the actual measured results obtained after fabricating the circuits. The simulated circuits have been implemented and sent for fabrication.

TPDL combinational logic gates have a maximum operating frequency of 2.38 GHz, while the static logic gates operate up to 1.2 GHz. The comparison in performance between all the designed TPDL and static logic gates is summarized in Table 1. The comparison between the speed of TPDL and static logic gates for different power supply voltages for NAND gates is shown in Figure 3. It is clear from this figure that the maximum operating frequency of the TPDL gates is more than double that for the static logic gates, when powered from the same supply voltage. Also, the power consumption of the TPDL gates is less than one-fourth that of the static logic gates when powered from the same power supply and driving the same load. This comparison holds true for comparison between static and TPDL 4-bit LFSRs or any other static and TPDL circuits performing the same logic function. For the power consumption comparison to be fair, the average consumed power of both TPDL and static circuits must be calculated at the same frequency. For example, from Table 1, the static NAND gate maximum frequency of operation is 1.2 GHz and the power consumption at that frequency is 5.8 mW, while the power consumed by the TPDL NAND gate at 2.38 GHz is calculated to be 1.98 mW. The fair comparison for the average consumed power, when both powers are calculated at 1.2 GHz, are 5.8 mW for the static gate and 1.4 mW for the TPDL gate when both gates are connected to the same power supply. However, the TPDL circuit will function properly at 1.2 GHz when powered from a 1.0 V power supply with much lower power

consumption. The average consumed power is then reduced to 0.15 mW. Therefore, at 1.2 GHz, the comparison between static and TPDL average consumed power will be 5.8 mW to 0.15 mW, which is over thirty-eight times.
Finally, the different designs are compared for their delay-power products. The comparison of power-delay products between the TPDL and static logic designed circuits at different power supply voltages is illustrated in Figure 5. The CGaAs TPDL power-delay product is less than one-tenth that of the static circuit performing the same function. CGaAs static circuits have about one-fifth the power-delay product compared to that of the comparable Si CMOS circuit performing the same function. This demonstrates one of the important advantages of TPDL over static logic.

The effect of increasing the load on the performance of the different designs is also studied and plotted in Figure . For the static circuits, the loads were static inverters. For the TPDL circuits, the loads were TPDL inverters. For the static circuits, the limiting parameter for the maximum frequency of operation is the propagation delay through the entire circuit. Increasing the load will increase the output capacitance of the circuit which increases the charging and discharging times of the output nodes. Therefore, the maximum operating frequency of the circuit decreases linearly with increasing output load. For the TPDL circuits, the load capacitance is separated from the output by a transmission gate. Thus, increasing the load capacitance will not increase the output capacitance. The limiting factor for the maximum operating frequency of the TPDL circuits is the charge redistribution. This problem is common to all dynamic logic circuits. Thus, TPDL circuits are less effected by increasing the output load.

5. CONCLUSIONS :

The results presented in this paper show that CGaAs TPDL circuits have more than double the operating frequency of static logic circuits performing the same function. Also, they dissipate less than one-fourth the power consumption compared to static logic when powered from the same supply voltage. CGaAs TPDL circuits have the lowest delay-power product ever reported in this technology (0.01mW/gate/MHz). TPDL GaAs circuits are excellent candidates for the next generation of high speed, high density and low power GaAs ICs such as DSP and digital communications ICs.

6. REFERENCES :

[1] Khaled Ali Shehata, "Low-power, high-speed dynamic logic families for complementary Gallium arsenide (CGaAs) fabrication processes" Ph.D. dissertation, Naval Postgraduate School, Monterey, California, September, 1996.

[2] Bruce Bernhardt et al, "Complementary GaAs: a high speed BiCMOS alternative" IEEE GaAs IC Symposium San Diego, Cal. Invited Paper, pp. 18-21, October 1995.

[3] Kevin R. Nary and Stephen I. Long "A 1 mW 500 MHz 4-bit adder using two-phase dynamic FET logic gates" IEEE GaAs IC Symposium, pp. 97-100, 1992.

[4] Khaled Ali Shehata, Douglas J. Fouts, "Complementary Gallium Arsenide low-power, high-speed dynamic logic circuit design" presentation at workshop on Complementary Heterostructure FET (CHFET) Technology, Albuquerque, New Mexico, November, 1996.

[5] Khaled Ali Shehata, Douglas J. Fouts, and Sherif Michael, "Dynamic Logic Families for Complementary Gallium Arsenide (CGaAs) Fabrication Processes" accepted for publication in IEEE Circuits and System Conference, Sacramento, pp. 1103-1106, August, 1997.

[6] Douglas J. Fouts, Khaled Ali Shehata, and Sherif Michael "A Dynamic Four-Bit Carry Lookahead Adder for Complementary Gallium Arsenide (CGaAs) Fabrication Processes" accepted for publication in IEEE Circuits and System Conference, Sacramento, pp. 1107-1110, August, 1997.

[7] Douglas J. Fouts and Khaled Ali Shehata, "Two-Phase Dynamc Logic Circuits for Gallium Arsenide Complementry HIGFET Fabrication" US Patent # 5926038, July, 1999.

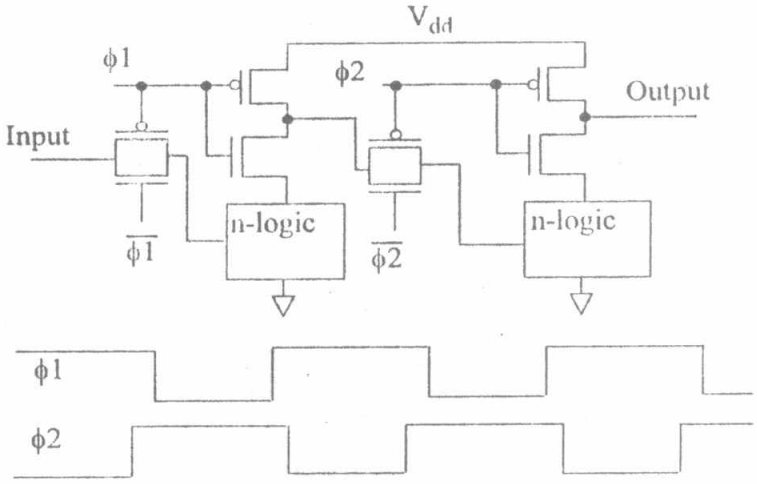

Figure 1: CGaAs TPDL Basic Circuit Topology

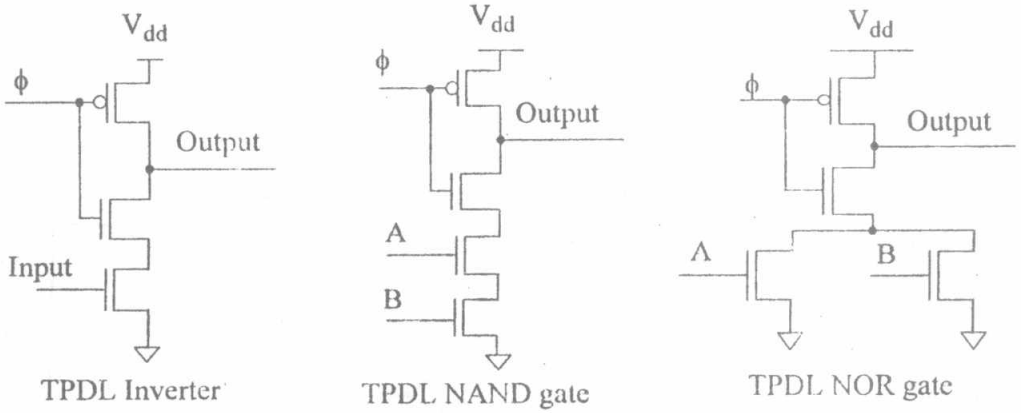

Figure 2: CGaAs TPDL Combinational Logic Gates

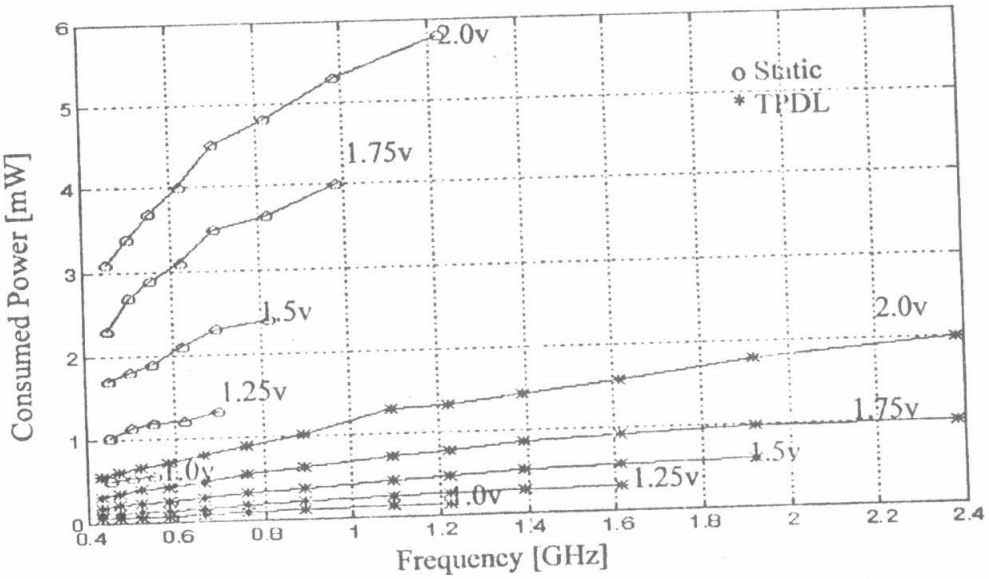

Figure 3: CGaAs Static and TPDL NAND Gate Power Consumption

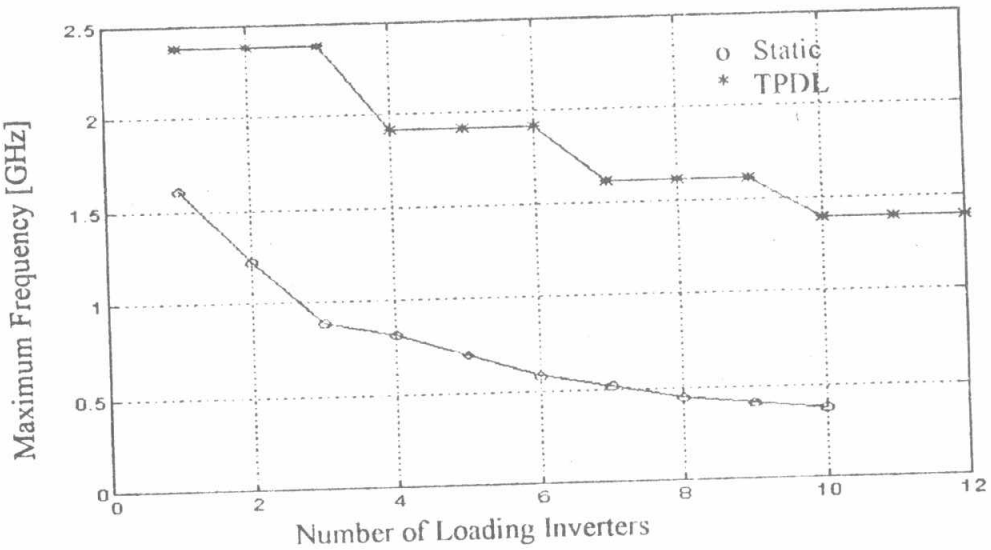

Figure 4: Loading Effects on CGaAs Static and TPDL NAND Gates

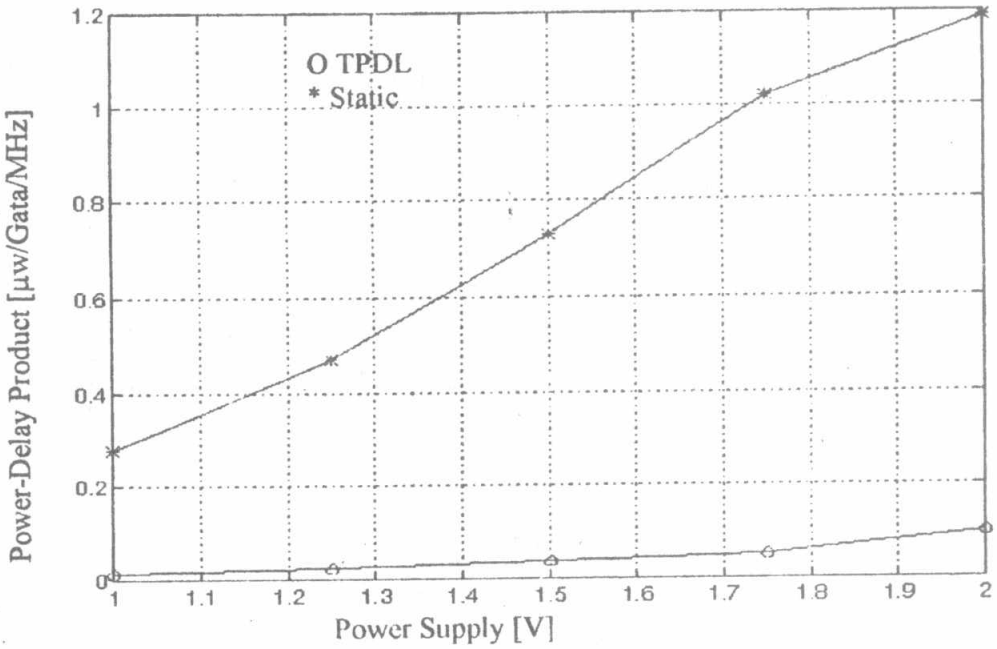

Figure 5: CGaAs Static and TPDL NAND Gate Power-Delay Product

TABLE 1: Comparison between CGaAs static and TPDL circuits.

Designed Logic Gate	Circuit Topology	Circuit performance		
		F_{max} [GHz]	P_{av} @ F_{max} [mW]	Number of Transistors
NAND	Static	1.2	5.8	4
	TPDL	2.38	1.98	4
XOR	Static	0.55 0.7	3.2 6.2	6 8
	TPDL	1.61	4.8	24
D Flip-Flop	Static	0.82	20.8	20
	TPDL	2.0	4.54	10
4-B LFSR	Static	0.55	48.2	88
	TPDL	1.2	15.89	54