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## **ANALYSIS AND DESIGN OF A MODIFIED GO-CFAR PROCESSOR. HARDWARE IMPLEMENTATION USING PLDs.**

FATHY\* M. ABDEL KADER, ALI\*\* M. ABOU ZEID, and NABIL\*\*\* GIRGIS M.

### **ABSTRACT**

Constant false alarm rate (CFAR) processors are useful for detecting radar targets in background noise for which all parameters of its statistical distribution are not known and may be non-stationary. The well known "Cell Averaging" (CA)-CFAR processor exhibits severe performance degradation in regions of abrupt change in the background clutter power. The "Greatest Of" (GO)-CFAR processor specially designed to control the false alarm rate during clutter power transition. A modification of the GO-CFAR processor is proposed. Analysis for the selection of the sampling rate, window length, word length, and multiplication factor is introduced. The proposed design gives an improvement in detection capability and resolution of decision with a great reduction in hardware complexity. A further reduction in hardware complexity is obtained by using programmable logic devices (PLDs). These devices increase the effectively of using software in hardware which, in turns, provide flexibility, modularity, expandability maintainability, and reduce size, cost, time and effort.

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\*Post graduate student, Main Workshops for Radar Equipment, Cairo, Egypt

\*\*Dr., Technical Research Center of the Armed Forces, Cairo, Egypt

\*\*\*Associate professor, Dpt. Of Radar and Guidance. MTC, Cairo, Egypt.

## INTRODUCTION

The signal returns from radar targets are usually buried in thermal noise and clutter, which refers to any undesired signal echo that is reflected back to receiver by buildings, clouds, the sea, etc. Since the clutter plus noise power is not known at any given location, a fixed threshold detection scheme cannot be applied to the radar returns in individual range cells if the false alarm rate is to be controlled. An attractive class of schemes that can be used to overcome the problem of clutter are the *constant false alarm rate* (CFAR) processing schemes which set the threshold adaptively based on local information of total noise and clutter power. The threshold in a CFAR detector is set on a cell by cell basis using estimated noise power by processing a group of reference cells surrounding the cell under investigation. An example of such a processor is the Cell Averaging (CA) CFAR processor, which adaptively sets the threshold by estimating the mean level in a window of  $M$  range cells. The CA-CFAR processor is the optimum CFAR processor (maximizes detection probability) in a homogeneous background when the reference cells contain Independent and Identically Distributed (IID) observations governed by an exponential distribution [1-2]. As the size of the reference window increases, the detection probability approaches that of the optimum detector, which is based on a fixed threshold.

One major problem suffered by a CA-CFAR processor presented by regions of clutter power transitions or edges and causes two different effects [2] :

- a) If the cell under test is in the clear region but a group of the reference cells are immersed in the clutter edge, a masking effect results. The threshold is raised unnecessarily and therefore  $P_d$  (along with  $P_{fa}$ ) is lowered significantly, even though there is a high signal to noise ratio ( $S/N$ ) in the cell of interest. Thus with CA-CFAR the clutter regions are actually expanded at each edge by about a half-length of the reference window ( $M/2$ ).
- b) On the other hand, if the test cell is immersed in the clutter return but some of the reference cells are in the clear, then  $P_{fa}$  increases intolerably with an increase in the interference level discontinuity. (A 20 dB discontinuity amounts to 3 to 4 orders of magnitude in  $P_{fa}$  [1-4]).

Modifications of the CA-CFAR schemes have been proposed to overcome the problems associated with non-homogeneous noise backgrounds. These schemes split the reference window into leading and lagging parts symmetrically about the cell under test. The noise power is no longer estimated efficiently, and therefore, some loss of detection in the homogeneous reference window is introduced compared with the CA-CFAR processor. Hansen [4] has proposed a CFAR procedure to regulate false alarm rate in the region of clutter transition; in this procedure the noise power is estimated by the greatest of (GO) the sums in the leading and lagging windows. The additional loss of detection performance (in terms of signal to noise ratio) over the CA-CFAR procedure in homogeneous reference window is typically found to be between 0.1-0.3 dB [5]. Moore & Lawrence [6] have shown that during clutter power transitions, a minor increase can be expected in the false alarm rate of the GO-CFAR processor in the worst case when the lagging window contains radar returns from the clear background while the leading window contains returns from the high clutter region. This is simply because the processor includes only the clutter samples

present in the window to estimate the noise power in the worst case. However, the GO-CFAR detector is incapable of resolving closely spaced targets. Weiss [3] has shown that detection probability decreases intolerably when a single interfering target with strength equal to that of the primary target appears in the reference window. However, the block diagram of the GO-CFAR processor is shown in Fig.1.

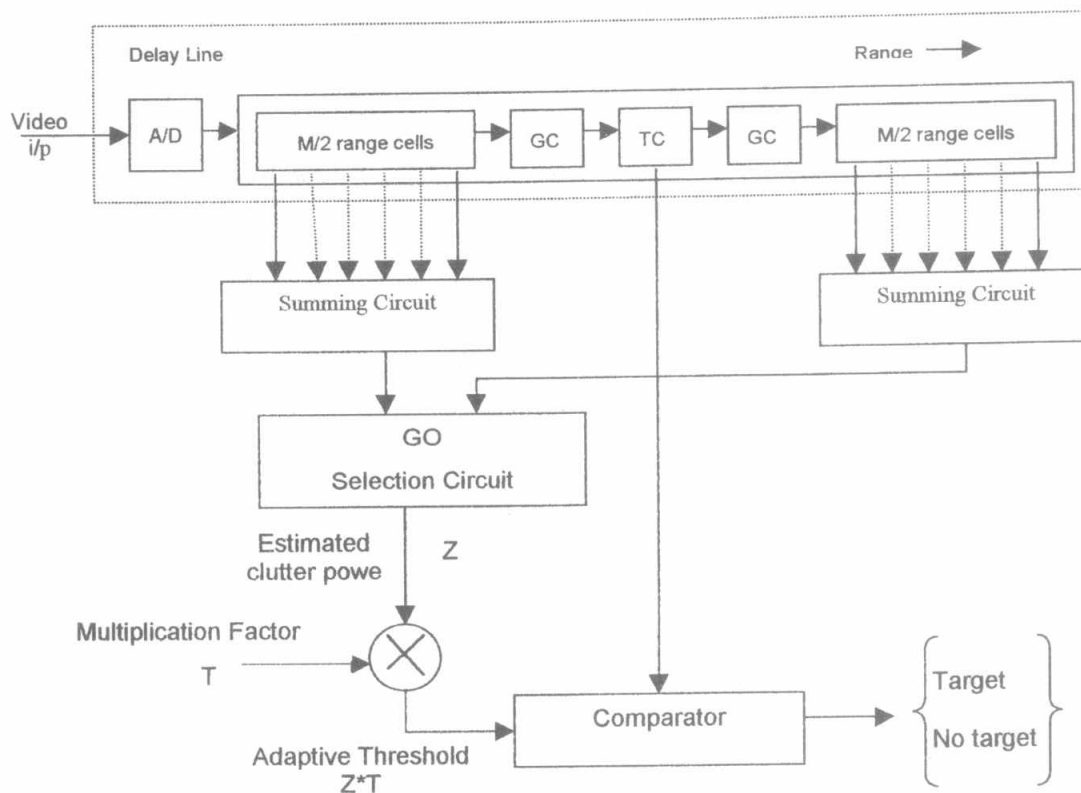


Fig.1 Block diagram of a GO-CFAR processor

As shown in this figure, the detected video range samples after the analog to digital converter are sent serially into a shift register of length  $(M+3)$  stages (delay line) which is divided into leading window of length  $M/2$ , lagging window of length  $M/2$ , two guard cells (GC), and the cell under test (TC). The estimated total noise plus clutter power is obtained by summing the samples in both leading and lagging windows by the summing circuits shown. The greatest of them is selected, then multiplied by a constant scale factor used to achieve a desired false alarm probability corresponding to the size of the used window. Comparing the result of multiplication (adaptive threshold) to the value present in the test cell. A target is declared to be present if the value in the test cell exceeds the threshold value.

## FACTORS AFFECTING THE REALIZATION OF THE GO-CFAR PROCESSOR

There are some factors must be considered and analyzed before realization of the GO-CFAR processor of Fig1. These factors are discussed in the following subsequent sections.





## Sampling Rate Selection

The sampling rate is selected according to Shannon theorem such that the radar range cell is covered by 4-successive samples. Since the accuracy of estimating the noise average power within the reference window increases as the number of samples increases, so representing the radar range cell by 4-successive samples will lead to a good representation of the analog video signal. Also the range resolution in taking the decision will be improved. The main disadvantage is the complexity of hardware. So, in the previous work [2] [3] [7], the radar range cell was represented by 1-sample to reduce the complexity of hardware.

The improved performance of the proposed GO-CFAR processor( 4-successive samples in each range cell ) is clear compared to the case of representing the radar range cell with one sample . However; Fig.2 shows the probability of detection at different probabilities of false alarm for two cases:

- i) 1 sample for the range cell
- ii) 4 samples for the range cell

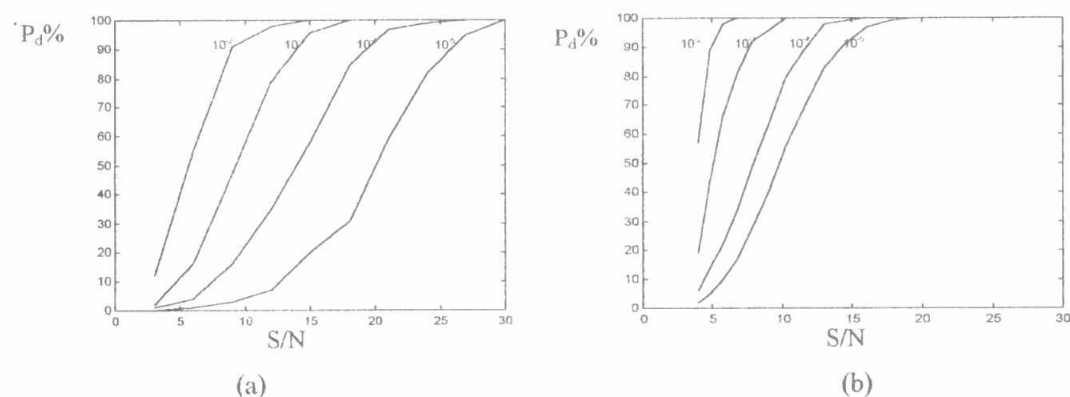


Fig.2 (a) The probability of detection at different probabilities of false alarm for the case (i)  
(b) The probability of detection at different probabilities of false alarm for the case (ii)

It's clear from this figure that the probability of detection over different probabilities of false alarm for case (ii) is better than that of case (i).

## Window Length selection

Selection of the window length was discussed in references [2],[3],[7] (a total of 4 up to 32 range cells was analyzed). Generally, as this length increases, the performance approaches that of the optimum detector, but on the other hand, the action of decision will not be sensitive to the fast changes. Also the hardware will be more complicated. Decreasing this length leads to a miss detection in case of multiple targets. In the present work, a moderate value for the reference window length is selected. Eight range cells (32 samples) for each of the lead or lag window are suitable.

However; Fig. 3 shows the effect of the window length selection on the probability of detecting a single or double targets in the reference window for the following cases:

- i) A window length of total 16 range cells.
- ii) A window length of total 8 range cells.

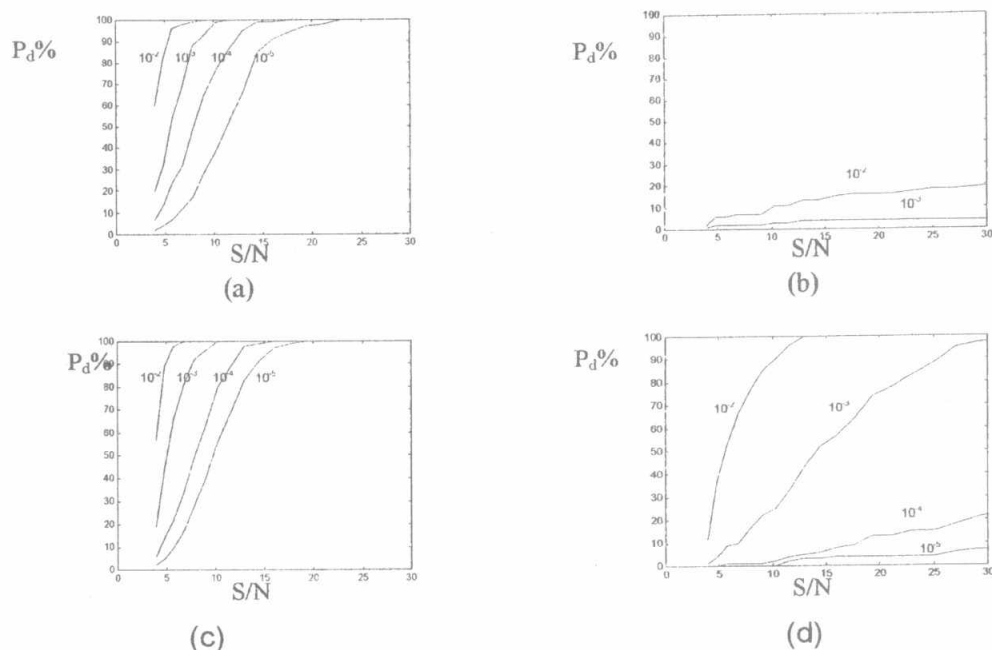


Fig.3 (a) The probability of detection at different probabilities of false alarm for a window length of 8 cells for one target  
 (b) The probability of detection at different probabilities of false alarm for a window length of 8 cells for two targets  
 (c) The probability of detection at different probabilities of false alarm for a window length of 16 cells for one target  
 (d) The probability of detection at different probabilities of false alarm for a window length of 16 cells for two targets

It's clear that as the used window length increases, the probability of detection increases. Also for the case of two targets in this reference window, the probability of detection of the extraneous target in the 16 cells window length is better than that of 8-cells window length.

The effect of the window length selection on the width of the output pulse in the case of extended length received signal (rain clutter, clouds, mountains, .....etc). is shown in Fig.4. It's clear that as the input pulse width increases, the output pulse width increases until a certain value and then begin to decrease till it reaches zero width. For the case of 8 cells window length, the width of the output becomes to decrease at values less than that of 16 cells window length. Since the width of input pulse expresses the change in clutter power so, the 8-cell is more sensitive to the fast changes.

A compromise between the high probability of detection and the required response due to fast changes in background level has to be obtained.

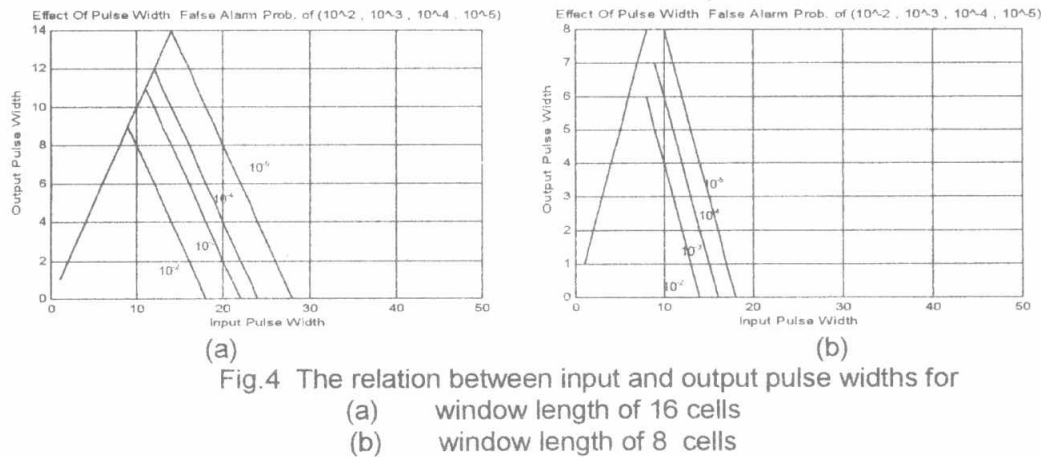


Fig.4 The relation between input and output pulse widths for  
(a) window length of 16 cells  
(b) window length of 8 cells

For the proposed GO-CFAR processor we use 16 cells window length to obtain a high probability of detection and a reasonable response due to change in background level.

### Multiplication Factor Selection

The selection of the multiplication factor depends on the total window length and the required probability of false alarm. Different values for this multiplication factors are obtained and shown in table 1 for two different window lengths.

**Table 1.** Constant multiplication factors of the proposed GO-CFAR Processor for different window lengths (M)

$P_{fa}$	M = 8	M = 16
$10^{-2}$	0.27	0.1
$10^{-3}$	0.33	0.13
$10^{-4}$	0.39	0.16
$10^{-5}$	0.45	0.21

### Word Length Selection

It's a well known fact that increasing the word length will lead to a better digital representation of the analog signal because of increasing resolution. But on the other hand, the hardware will be more complicated

A software simulation of the filter is used to demonstrate the effect of the word length on the obtained results. The simulated reflected target video echo is corrupted with Gaussian noise. The results are obtained for different signal to noise ratio (S/N) and for different signal amplitudes (compared to the reference voltage of the used analog to digital converter (A/D) which is considered to be +5 volts). These results (for  $P_{fa}=10^{-3}$ ) are shown in Fig.5.



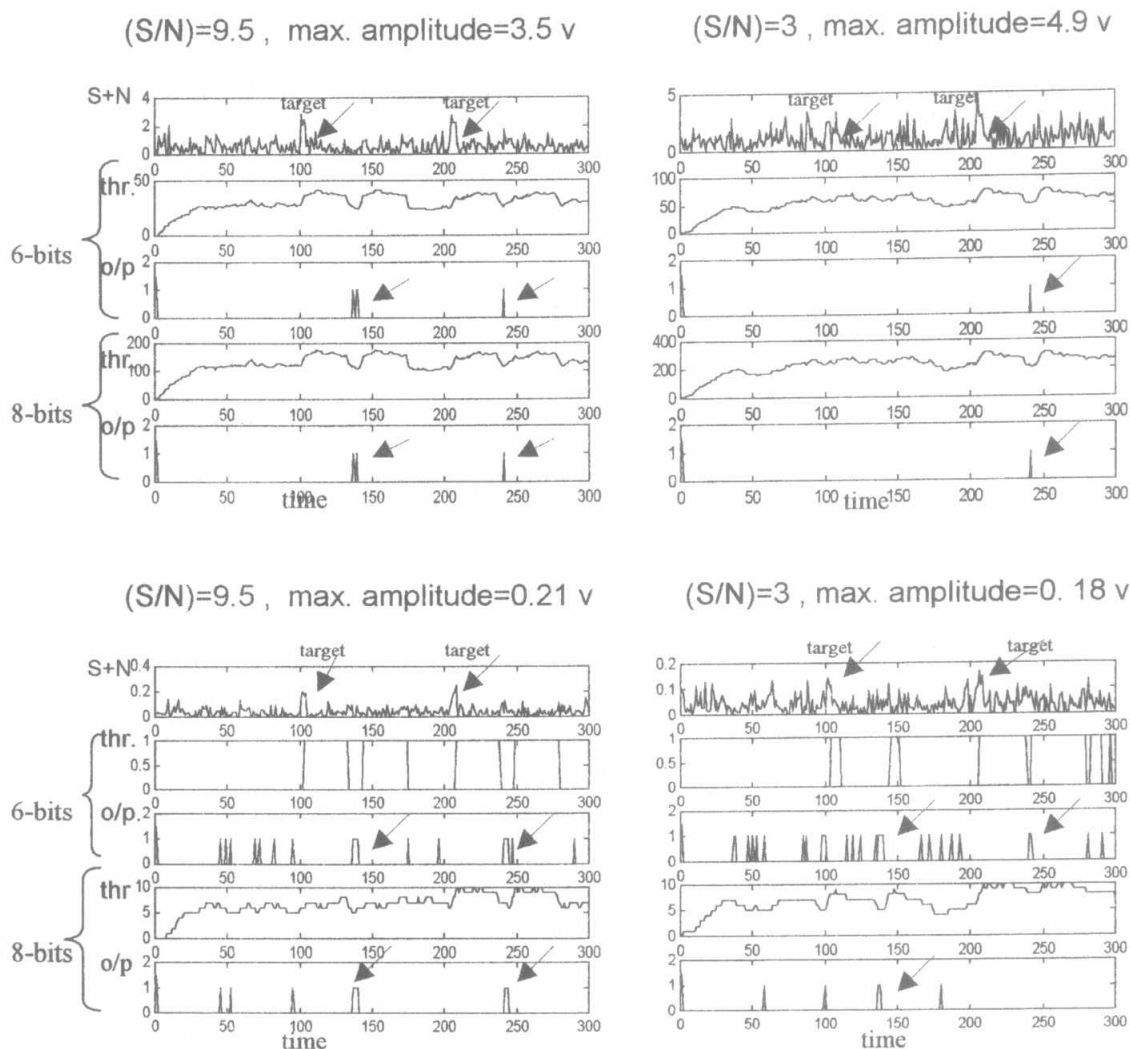


Fig.5 Effect of word length selection

Analysis of Fig.5 leads to the following results:

- The performance of the filter for both word lengths at a given (S/N) ratio becomes bad when the absolute amplitude of the signal plus noise is small compared to the A/D converter voltage range.
- The performance of the filter for the case of 8 bits word length is still better than that for the case of 6 bits word length when the absolute amplitude of the signal plus noise is small compared to the A/D converter voltage range.
- Generally, it is better to control the absolute input signal amplitude such that it covers the most range of the A/D converter.

The effect of the word length on the minimum detectable target signal ( $S_{min}$ ) and consequently on the minimum (S/N) is demonstrated on Fig.6. It is shown from this figure that, for both the 6-bits and 8-bits word lengths; the minimum detectable target signal ( $S_{min}$ ) increases as the noise rms voltage increases.

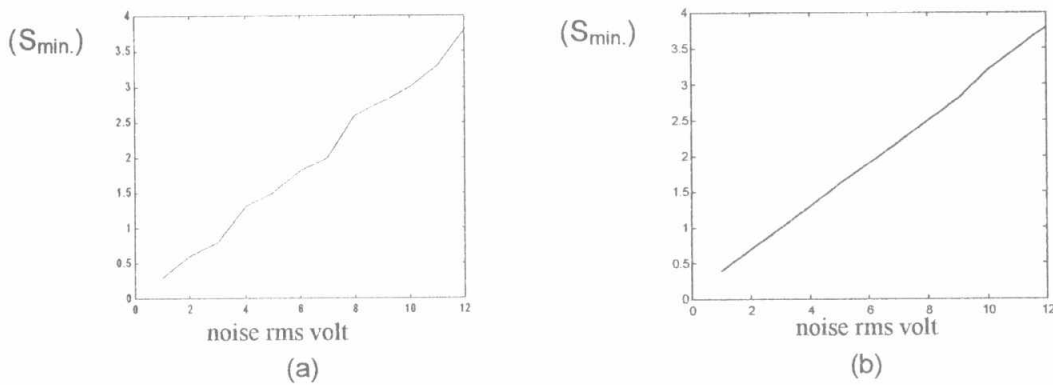


Fig.6 Effect of word length on the minimum detectable target signal ( $S_{min}$ ), ( $P_{fa}=10^{-3}$ )  
 (a) 6 bits word length  
 (b) 8 bits word length

The minimum signal to noise ratio ( $S/N$ ) required for detection at different noise levels oscillates around an average value. This oscillation is reduced for the 8-bits word length because of increasing the resolution of representing the video signal. However, as the number of bits increases, the performance is improved.

## THE RECURSIVE APPROACH OF THE MODIFIED GO-CFAR PROCESSOR IMPLEMENTATION

To realize the GO-CFAR processor shown in Fig.1 for the proposed modification (the radar range cell is represented by 4-successive samples) using the non-recursive approach [ Fig.7(a) ] for realizing the delay line and the summing circuits, a large number of chips is required (approximately 200 chips for the case of a range cell of 4-successive samples, each sample of 8-bits, and a total window length of 16-cells), which is a very large number makes the design very complex. So, an alternative method is proposed to realize the delay line and the summing circuits. Instead of adding the received samples in either lead or lag windows non-recursively to get the sum of the total samples, this addition will be performed recursively [Fig.7(b)] with maintaining the stability of the system.

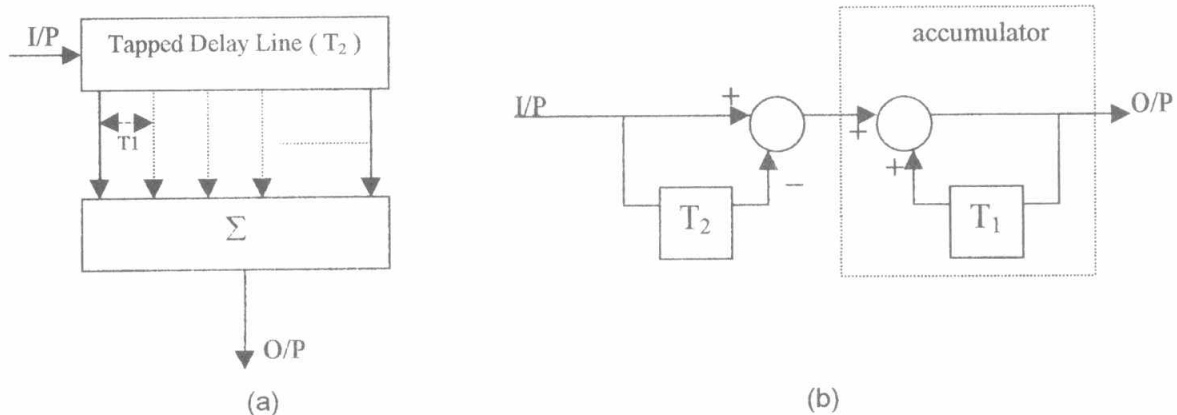


Fig.7 (a) non-recursive realization of addition  
 (b) recursive realization of addition

To realize the delay line and the summing circuits shown in Fig.1 using the recursive approach, a small number of chips (approximately 29 chips) is required. So, a great reduction in the hardware complexity is obtained compared to the complexity of the non-recursive realization.

## REALIZATION OF THE PROPOSED GO-CFAR PROCESSOR USING PLDs

A PLD is a digital integrated circuit capable of being programmed to provide a variety of different logical functions [8]. The use of these devices in the design leads to many advantages. These advantages include the reduction of part count, reduction of cost, reduction of testing requirements, and reduction of maintenance and repair [9]. These devices also provide and increase the software effectivity in system design, which in turns, provide flexibility, modularity, expandability, and maintainability. Many software languages are used for digital designing with PLDs. The Design Synthesis Language (DSL) as a famous, simple, and efficient language is used to design the proposed GO-CFAR processor. However, Fig.9 shows the block diagram of the designed GO-CFAR processor using (DSL). This block diagram is drawn as it is on a schematic page in the software.

The simplicity in designing using this language is clear compared to designing using discrete components. Only, we have to identify each block, write its procedure (program), identify each signal in the program as an input or output to the block, and connect lines and buses between blocks in the circuit under consideration. Compiling and running this software will result in fitting this design into the available PLDs. A list of all possible solution is displayed according to our priorities. Also we have the ability to simulate and test the design. For simplicity, the design of the proposed GO-CFAR processor will be implemented with 6 bits word length.

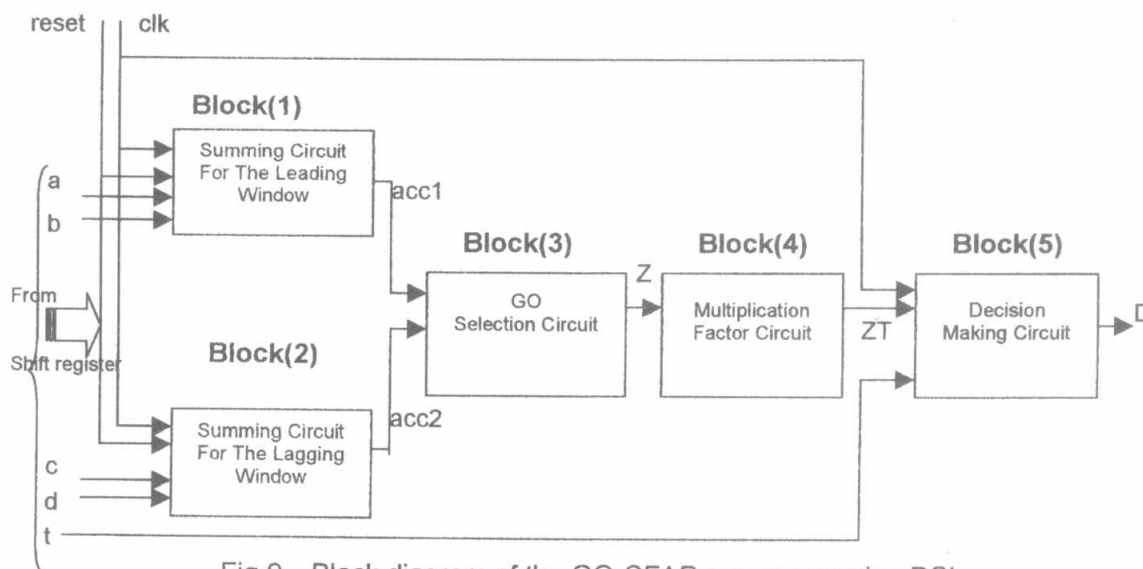


Fig.9 Block diagram of the GO-CFAR processor using DSL

Because of the availability of the PLD chips and the corresponding programmer, the design (block 1, block 2, block 3, and block 5) is fitted into 3-chips of a high density

PLDs with generic number ( ATV2500BQ-20DC ), which is a 40-pin DIP packaged chips.

The delay line is implemented using discrete components (shift register). Also, block 4 is implemented using an EPROM ( $2^{13} \times 8$ ). The most significant two bits of the address of the EPROM are used to select the value of the multiplication factor corresponding to one of the probabilities of false alarm ( $P_{fa}$ ).

So, the total number of the used chips is 14 chips; 3-PLDs chips (ATV2500BQ-20DC), single EPROM, single hex-inverter, and 9-chips of shift register.

The great reduction in the hardware complexity is obviously clear now. This is beside to the simplicity in design, reduction of time, reduction of size, and reduction of cost. All these are additional advantages of the present realization.

## RESULTS AND MEASUREMENTS

The implemented GO-CFAR processor using PLDs is tested experimentally for the following cases:

- 1- The effect of input pulse width (rain clutter, clouds, mountains,... etc) on the output pulse width for different probability of false alarm.
- 2- The minimum ( S/N ) required for detection at different noise rms voltages for different probabilities of false alarm.

For the case number (1), Fig.10 shows the measured values of the output pulse widths for different input pulse widths at different probabilities of false alarm. The sampling rate is  $f = 1$  MHZ. The measured results are found to be identical to those theoretical values of Fig.4.

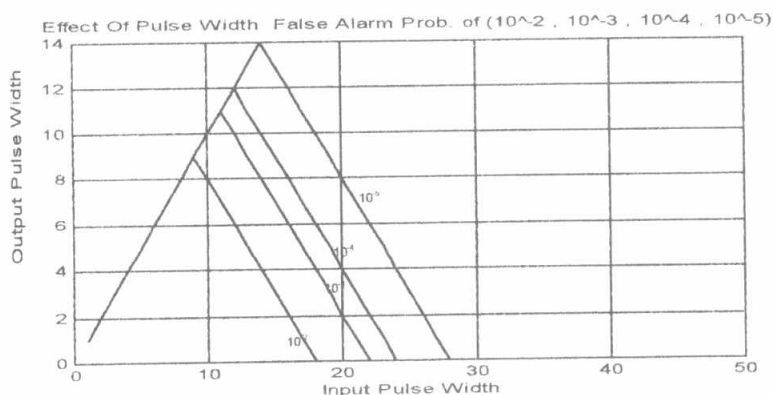


Fig.10 Measured values of the output pulse widths for different input pulse widths at different probabilities of false alarm. (the sampling rate is  $f = 1$  MHZ)

For the case number (2), Table 3 shows the measured values of the minimum detectable target signal ( $S_{min.}$ ) and the corresponding  $(S/N)_{min.}$  at different noise rms voltages for different probabilities of false alarm.

**Table 4** Measured values of the minimum detectable target signal ( $S_{min}$ ) and the corresponding  $(S/N)_{min}$  at different rms noise values for different probabilities of false alarm.

Noise rms voltage	$P_{fa}=10^{-2}$		$P_{fa}=10^{-3}$		$P_{fa}=10^{-4}$		$P_{fa}=10^{-5}$	
	$S_{min}$	$(S/N)_{min}$	$S_{min}$	$(S/N)_{min}$	$S_{min}$	$(S/N)_{min}$	$S_{min}$	$(S/N)_{min}$
0.2	0.47	5.50	0.65	10.50	0.80	16.00	1.20	36.0
0.4	0.80	4.00	1.30	10.56	1.50	14.06	3.20	64.0
0.6	1.20	4.00	2.10	12.25	2.80	20.25	4.40	53.7
0.8	1.80	5.06	2.80	12.25	3.00	14.00		
1.0	2.20	4.85	3.10	09.60	4.00			
1.2	2.70	5.06	3.90	10.60				
1.4	3.10	4.90						

Note: For the small values of  $P_{fa}$ , the value of the rms noise voltage plus target signal ( $S_{min}$ ) exceeds the range of the used A/D converter.

The measured values are found to be very close to the values calculated theoretically [ For example, for the case of  $P_{fa}=10^{-3}$  of Fig.6 ]

## CONCLUSION

A CFAR processing is widely used in digital radar systems to control false alarm rate. The basic CA-CFAR processor was found to suffer from some problems. A GO-CFAR processor is designed specially to overcome the problem of clutter power transitions.

Analysis for the selection of the sampling rate, window length, word length, and multiplication factor with a modification of the GO-CFAR processor are introduced.

Three modifications of this processor were introduced; namely:

- 1- Improving the detection capability and decision resolution by increasing the sampling rate (representing the radar range cell by 4 successive samples instead of one sample as in previous work).
- 2- Reduction of hardware complexity if discrete components are used (from 200 chips to 29 chips) which is a great reduction results in realizing the delay line and the summing circuits recursively instead of non-recursive realization with maintaining the stability of the system.
- 3- Using **PLDs** in implementation leads to a more reduction in hardware complexity ( total number of the used chips is 14 ), and a more simplicity in design.

All the above proposed modifications lead to an improvement in performance with a great reduction in size, time, effort, cost. Also increasing of flexibility, modularity, expandability, and maintainability of the design.

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